Remarks

Reconsideration of the application is requested. Applicants respectfully traverse the rejections of claims 1, 5, 15, 19, 22, and 27-30 as anticipated by Anderson and claims 7, 8, 11, 12, 14, 21, and 23-26 as unpatentable over Anderson in view of Aung.

Applicants have amended claims 1, 8, and 15 to correct the informalities noted by the Examiner. Applicants have also amended claims 22, 27, and 29 to clarify their meaning. These claim amendments are purely to the form of the claims and are not intended to narrow their scope.

The § 102(b) Rejections

Claim 22 recites, among other things:

> a phase interpolator coupled to a multiplexer responsive to the FWD and BWD signals, the multiplexer operable to receive a plurality of given clock signals having different phases as inputs and to select each of at least two clock signals as outputs, the phase interpolator operable to generate a recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals

This arrangement, in which the multiplexer first selects a pair of given clock signals and the phase interpolator then interpolates between them, requires that only one phase interpolation be done. Similar limitations in structure and method are recited in independent claims 1, 8, 15 and 27-29.

In contrast, Anderson discloses a different approach. With reference to Figs. 3 and 4 and col. 3, line 32 to col. 4, line 12, it can be seen that Anderson first interpolates all of its given clock signals to provide a much larger number of clock phases. This, of course, requires providing more phase interpolators than required by the claimed invention, with all of the consequent disadvantages of increased size, complexity, and power consumption. Anderson then selects from among these clock phases using a multiplexer (Fig. 9; col. 5, lines 15-25. This is essentially opposite to the approach of the claimed invention.

The Examiner points to synthesizer 208 (and by extension to its preferred embodiment in Fig. 8) as being the claimed multiplexer. This is not the case.

Synthesizer 208 (col. 2, lines 50-55) is merely the source of the given clock phases (i.e., signals). Fig. 8 shows in more detail that the synthesizer is not a multiplexer, nor that it is responsive to the FWD and BWD signals.

Anderson cannot thus be said to anticipate the claimed inventions, for at least the reason that it does not disclose the claimed arrangement of multiplexer and phase interpolator.

The § 103(a) Rejections

As noted above, Anderson (the primary reference for this rejection) advocates the opposite approach to what is claimed. Whereas Anderson teaches interpolating each and every given clock signal and then selecting from among those interpolated signals, applicants' claims recite selecting from among the given clock signals and then interpolating the selected signals. Applicants believe that their approach is superior because it minimizes the number of phase interpolators and thus avoids the above-mentioned disadvantages of a multiple interpolator approach.

Anderson cannot thus be said to teach or suggest what is claimed. Aung adds nothing to Anderson in this respect.

For the reasons stated above, applicants submit that the claims are not anticipated by the prior art and that the prior art does not establish a prima facie case of obviousness. Applicants believe that the present claims are in now in condition for allowance, and such action is respectfully requested.

Please call the undersigned if he can be of any assistance in this case.

Respectfully submitted,

Date: 6/8/05

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